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Design & Simulation Of High-Performance Photovoltaic Module-Integrated Converter (PV-MIC)

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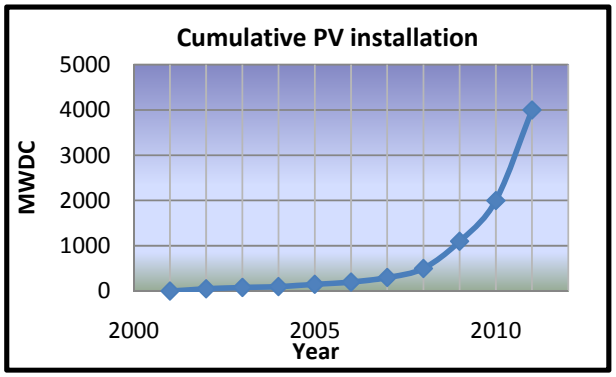
ABSTRACT

The paper present a single-phase grid-connected transformer less photovoltaic (PV) module-integrated converter (MIC) based on cascaded quasi-Z- source inverters (qZSI).In this system ,each qZSI module serves as an MIC and is connected to one PV panel .Due to the cascaded structure & qZSI topology ,the proposed MIC features low-voltage gain requirement , single-stage energy conversion ,enhanced reliability & good output power quality. Optimized module design is developed based on the derived qZSI ac equivalent model And power loss analytic model to achieve high efficiency and high power density .A design example of qZSI module is presented for a 225 to 250-Watt PV panel with 22-50 o/p Voltage . The simulation & experimental resultwhich prove the validity of analytical models. The final module prototype design achieves up to high efficiency with 100 kHz switching frequency. The peak efficiency can be further improved with synchronous rectification. Though the transformer less CMI based PV systems can achieve high performance and low cost.

KEYWORDS:MIC,qZSI ,eGaN FETs ,PV system,CMI

I. INTRODUCTION:

The grid-connected photovoltaic (PV) generation system markets are growing rapidly due to the environment concerns and government incentives. The cumulative installation of the grid connected PV systems in U.S. from 2001 to 2011 is shown in graph1. The total installed grid-connected PV system capacity was increased to 4GW in 2011.The capacity of PV systems installed in 2011 is 1.845 MWDC, was more than ten times the capacity of PV installed in 2007[1].



Graf 1.Cumulative U.S. grid-connected PV installations from 2000 to 2010.

The PV system cost can be broken down into three parts: the PV modules, the PV-inverter, installation and the remaining balance of system costs.

Table 1: Typical module prices from 1995 to 2011.

Year	1995	2005	2009	2011
Standard module price(s): USD/W	$5.01	$3.65	$2.82	$1.67
Best price for Large quantity buyers, USD/W)	$4.90	$3.03	$2.18	$1.28

For large use of PV–System Great effort is needed to reduce the cost of PV- System. the average price of PV modules decreased dramatically in these years as indicated in Table 1.With evolving technologies, the goal of $1 per watt PV cell can be achieved in the near future if the cells are manufactured at a large scale[1].

II. RELATED WORK:

This paper presents a grid-connected PV MIC based on cascaded quasi-Z-source PV inverters, as shown in Fig. 2. The reason of using qZSI instead of ZSI is that the required capacitance of the passive network can be largely reduced. In addition, a modified modulation strategy based on saw tooth carrier method is used to improve the system efficiency under boost operation mode[3]. The enhancement mode gallium nitride field-effect transistors (eGaN

FETs), which have emerged as promising next-generation power switches, are applied in the inverter. In order to achieve high performance of the proposed inverter, the design of a qZSI module needs to be optimized first. Therefore, the ac equivalent model of a qZSI is derived to help obtain the current and voltage information of the passive components and active switches. The power loss analytical model is then developed to evaluate the system efficiency.

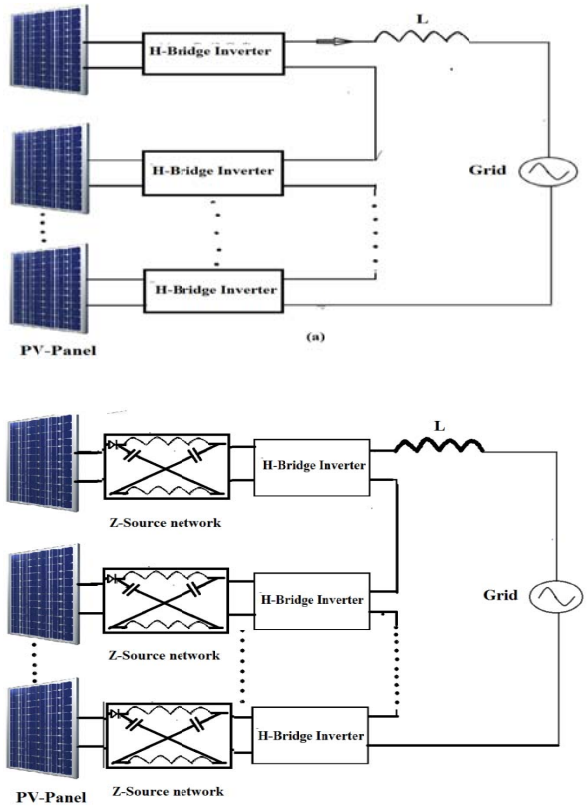


Fig.1.Gird-connected PV MIC configurations based on (a) cascaded H-bridge inverters and (b) cascaded ZSIs.

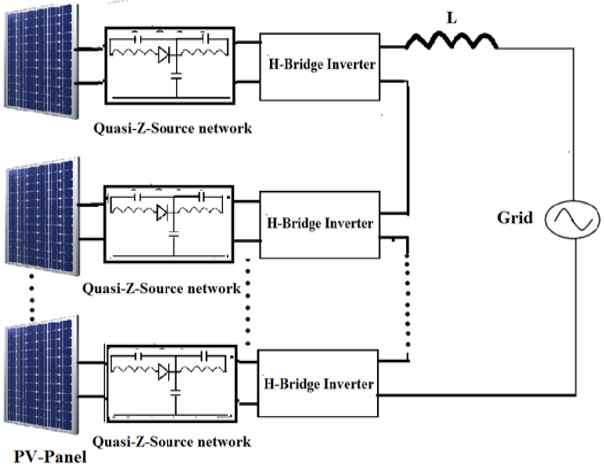


Fig. 2. Proposed gird-connected PV MICs based on cascaded qZSI.

Based on the two analytical models, the qZSI module is optimized to achieve high system efficiency and high power density[2]. The proposed design method can provide the optimal number of cascaded modules, the inverter switching frequency and the quasi-Z-source network parameters for different selected PV panel.

Topology Selection in ZSI Family :-

All the inverters of the voltage-fed ZSI family have the boost and shoot-through functions. This section compares these inverters regarding the required capacitance of the passive network, since the major difference among the different topologies is the voltage rating of the Z-source capacitors. The voltage-fed ZSI family includes the traditional ZSI, qZSI, and qZSId. The LC network configurations of the three topologies are shown in Fig. 3. [1]

Table 2
Voltage Rating Of The Capacitors

	Vc1	**Vc2**
ZSI	———Vin	———Vin
Qzsi	———Vin	———Vin
qZSID	———Vin	———Vin

Because the energy stored in the capacitor is proportional to the square of the across voltage and its capacitance, the lower capacitor voltage results inhigher capacitance to buffer the same amount of energy[1][2][6].

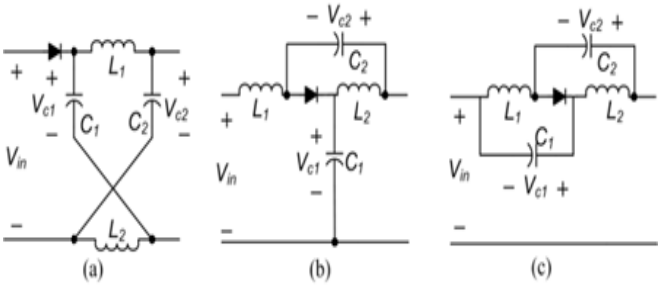


Fig. 3 LC network configurations of voltage-fed Z-source inverter family (a) ZSI; (b) qZSI; and (c) qZSId.

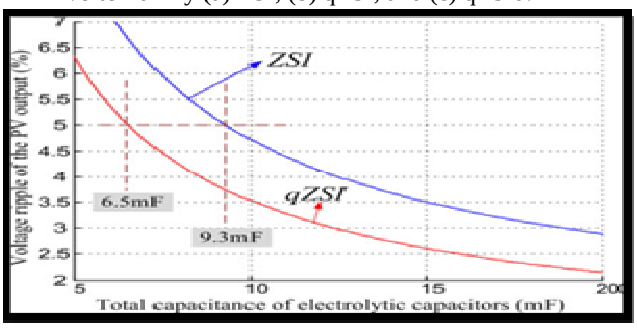


Fig. 4. Relationship between the total required electrolytic capacitors and the PV voltage ripple for ZSI and qZSI.

III. WORKING:

The Z-Source inverter having three operating mode.

(a) active state,

(b) zero state, and

(c) shoot-through state.

Below fig.5 show all the three state of operation

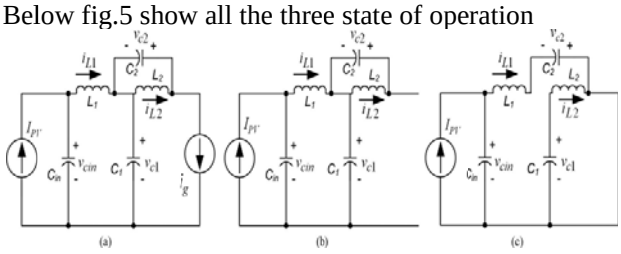


Fig. 5. Different operation modes of the qZSI(a) active state, (b) zero state, and (c) shoot-through state.

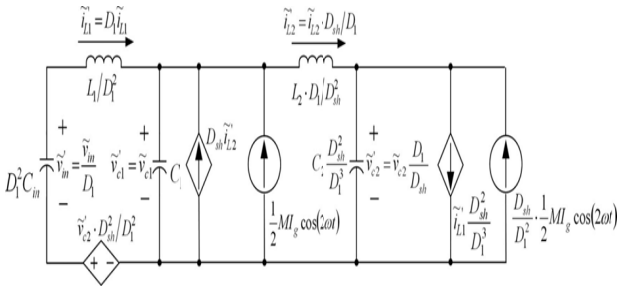


Fig. 6.AC equivalent circuit model of the qZSI.

During Buck & Boost Operation Switching Sequence of Inverter bridge are change which is explain in Table3.

Table 3.

Switching sequences of the full bridge in each switching cycle for (a) buck mode and (b) boost mode.

Switch / Period	S1	S2	S3	S4	State
T_0-T_1	on	off	on	off	Zero
T_1-T_2	on	off	off	on	Active
T_2-T_3	off	on	off	on	Zero
T_3-T_4	on	off	on	off	Zero
Switching events(on/off	2	2	2	2	

(a)buck mode

Switch / Period	S1	S2	S3	S4	State
T_0-T_1	on	on	on	on	Shoot-through
T_1-T_2	on	off	on	on	Zero
T_2-T_3	on	off	off	off	Active
T_3-T_4	off	on	off	on	Zero
T_4-T_5	on	on	on	on	Shoot-through
Switching events (on/off)	2	2	2	2	

(b)boost mode.

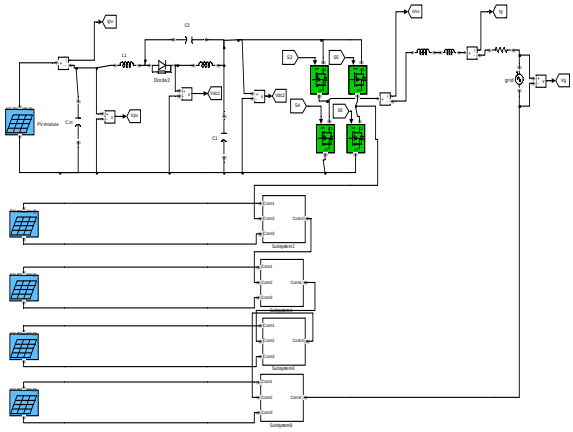


Fig. 7. Configuration of the proposed PV MICs based on cascaded qZSIs.

Particularly, when the inverter does not operate in boost mode, thatis, Dsh = 0, Vc1 and Vc2 of qZSId equal to zero, so they cannot buffer any double-frequency power. Therefore, the qZSId is not appropriate for the single-phase application[1][7]. For the ZSI, both C1 and C2 use electrolytic capacitors due to the same voltage rating of them. For the qZSI, electrolytic capacitor is only used for C1 due to its higher voltage rating than C2. Fig. 4 shows the relationship between the total required electrolytic capacitorsand the PV input voltage ripple for both ZSI and qZSI. The curve is obtained based on the ac equivalent models of ZSI and qZSI. The derivation of ZSI ac equivalent model can be found in and the one of qZSI will be given in Section III. It is evident that the qZSI requires less electrolytic capacitors. For example, when the PV voltage ripple is designed to be 5%, the required capacitance of electrolytic capacitors for qZSI is 30% less than ZSI. Therefore, the qZSI is selected[2][8].

Cascaded qZSIs With Modified Modulation Strategy:-

The configuration of the grid-connected PV inverter based on cascaded qZSI modules is presented in Fig. 5. Each qZSI module is installed on the backside of a PV panel. The eGaNFETs are applied as the power switches. The parameters of the quasi-Z-source network, inverter switching frequency, and cascaded module number will be obtained through an

optimization procedure given in Section. In the cascaded bridge structure, since each PV input is not grounded, several resonant paths are formed by the parasitic capacitances between the PV panels and the ground, the output filter *Lg*, and the inductance of interconnection cables between different bridges[2][5].

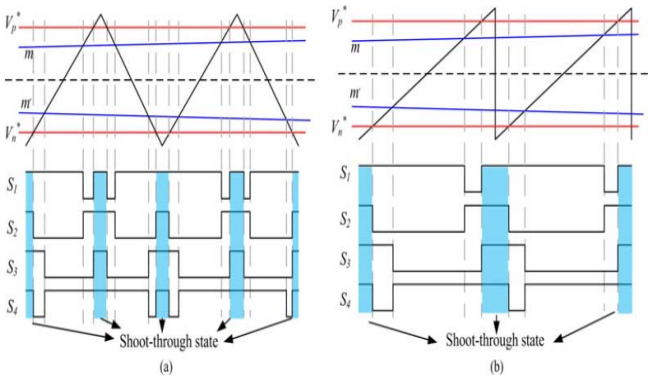


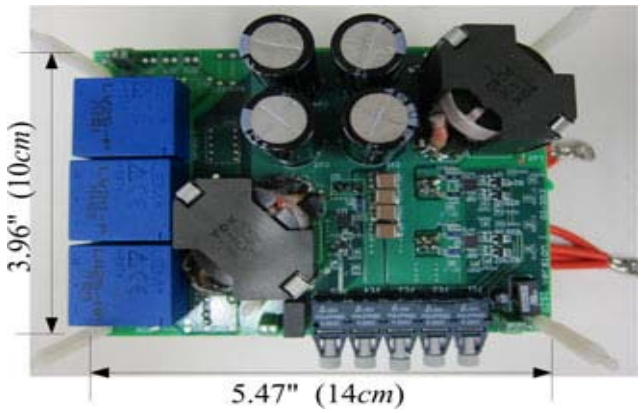
Fig. 8. Modulation strategies for qZSI (a) traditional method based on triangular carrier and (b) proposed method based on saw tooth carrier.

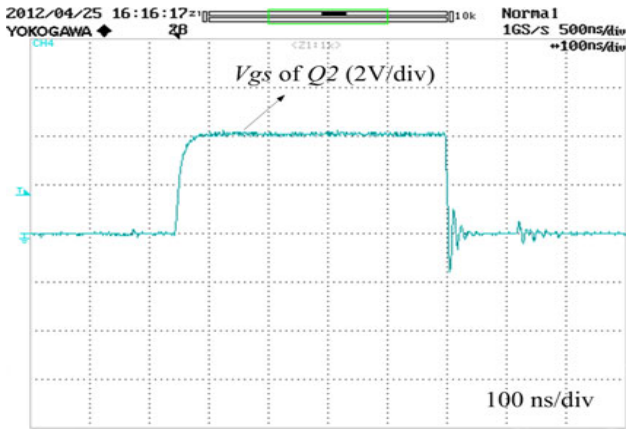
III. DESIGN OPTIMIZATION:. PROTOTYPE AND EXPERIMENTAL RESULTS

We study The 250-W qZSI module prototype& it's experimental result Which is given below.

A. qZSI Prototype ;-

The 250-W qZSI module prototype was built based on the optimized design, as shown in Fig. 13. The input voltage of thismodule is from 25 to 50 V. It is constructed on a four-layer PCB, integrating the quasi-Z-source network, the full bridge, the driver circuit, and sensors[3][9].





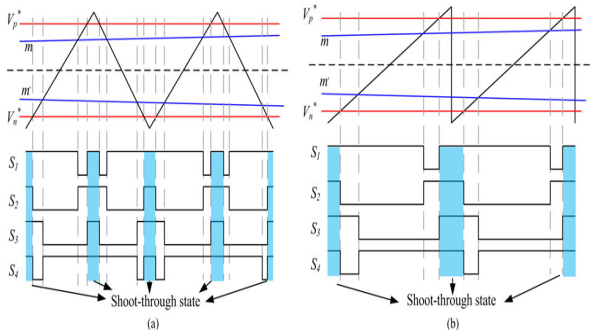


Fig. 9.qZSI module under test.&Fig. 14.Gate drive voltage of *S*2 at 45-V and 44-W input.

The design of the eGaN FET drive circuit needs to consider the device's ultralow threshold voltage and absolute maximum gate voltage rating. The minimum threshold voltage can be as low as 0.7 V and the maximum gate voltage rating is 6 V forthe selected EPC2001 eGaN FET. Considering the qZSI devices immunity to shoot through, the ultralow threshold voltage which may cause unintended miller turn-on will not be the concern. However,the overshoot of the gate voltage during turn-on process needs to be limited to guarantee the gate voltage not to exceed 6 V. In order to minimize the gate overshoot, the stray inductance in the driver circuit loop should be decreased. Detailed guidelines of decreasing the stray inductance in the driver circuit loop can be referred to. The LM5113 half-bridge driver in an leadless leadframe package (LLP) package is used to drive the eGaNFETs . The turn-off resistor is 0 Ù to make fast turn-off process, while the turn-on resistor is chosen as 5.1 Ù to further limit the possible gate overshoot. Fig. 14 shows the gate drive voltage of S2 at 45-V and 45-W input condition. There is no overshoot on the gate voltage during the turn-on transient.At higher power ratings, no overshoot is observed either. Overshoot is observed on S2 gate voltage, when S2 is ON and S1 is switched toON-state for shoot-through state. The large di/dt in the power loop couples into the gate

loop through thecommon source inductance. However, the overshoot is always below 6 V. For the qZSI, there is no dc capacitors right across the fullbridgedc link. The length of the high-frequency power loop, highlighted in Fig. 10(a), is longer than that of the traditional H-bridge with decoupling capacitors placed right across the dc link. Because of the longer high-frequency loop, the overshoot on the devices will be larger. One way to limit the over shootis through layout optimization. Another effective solution isto use a dc rail clamp circuit . In this paper, the layout optimization is performed. In order to reduce the loop strayinductance, *L*1, *L*2, *C*1, *C*2,*D*1and the full bridge are placed close to each other. In the layout design, bus 1–4 in Fig. 10(a) are formed using copper polygon in different layers and there is overlap between each other, so the spatial area looped by the high-frequency power loop will be small. Therefore, the loop stray inductance can be reduced. The PCB layout of the high-frequency power loop is shown in Fig. 10(b).

B. Experimental Results;-

The 250-W qZSI module was tested at 40, 45, and 50-V input under different power conditions. The module output voltage amplitude is 42 V as N is selected to be 4. The emphasis of this paper is the module efficiency, so the control of qZSI was openloop and the resistance load was used.

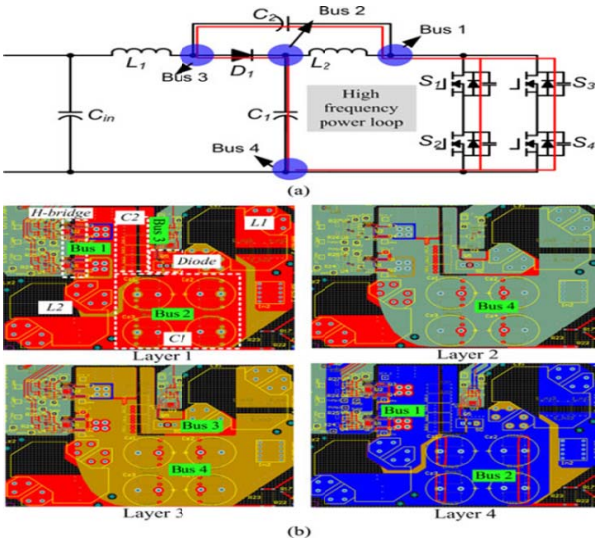


Fig. 10. High-frequency power loop in the qZSI: (a) schematic and (b) PCB layout.

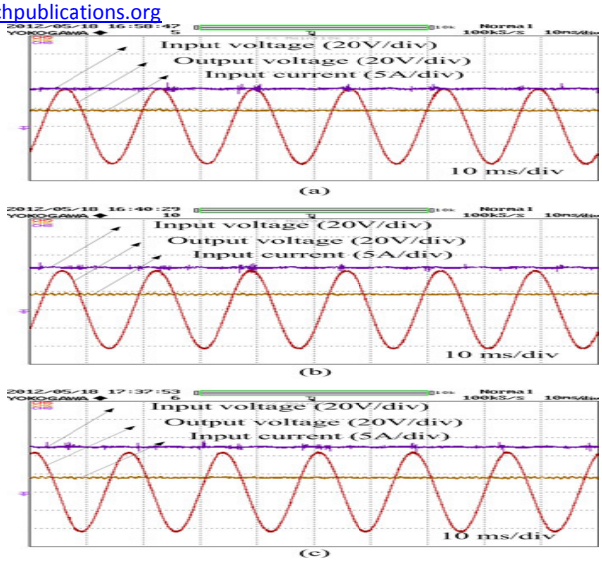


Fig. 11.Experimental waveforms of the qZSI module at 180 W under (a) 40-V input, (b) 45-V input, and (c) 50-V input.

Fig. 11 shows the qZSI input and output waveforms under the three input voltage levels at 180W[6][10]. When the input voltage VPV = 45Vand VPV = 50V, the qZSIoperated in buck mode; when VPV = 40V, the qZSI operated in boost mode. The measured efficiency curves of the module at three input voltage levels are provided in Fig. 12. The module efficiency was measured using the digital power analyzer, YokogawaWT3000. The results show that when the input power was higher than 50 W, the system efficiencies were above 97%. The peak efficiency 98.06% was achieved at 45-V, 140-W input condition.The measured efficiency of 40-V input and 45-V input are compared with their calculated results in Fig. 13. The consistence between the measured and calculated efficiencies verified the derived ac equivalent model and power loss analytical model of the qZSI. It also proved the effectiveness of the optimization procedure.

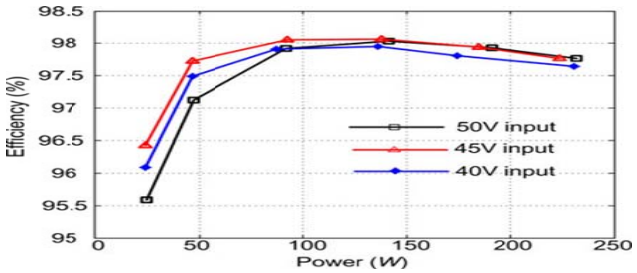


Fig. 12.Measured qZSI module efficiency curves at 40, 45, and 50 V.

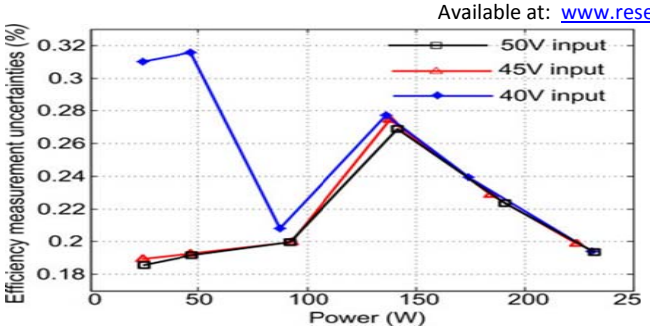


Fig. 13.Uncertainties of the module efficiency measurement.

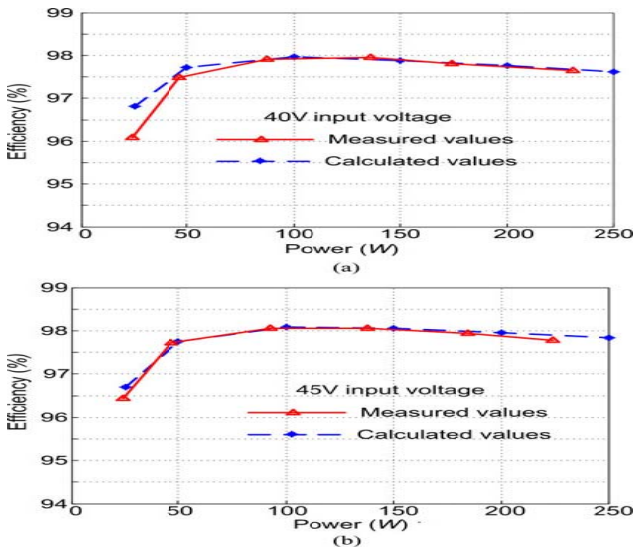


Fig. 14.Comparison of the measured andcalculated efficiencies for (a) 40-Vinput, and (b) 45-V input.

Discussion of the Results :-

Since the MIC is attached on the backside of PV panel, it suffers high ambient temperature. Due to the cost and waterproof requirements, the MIC cannot be fan cooled so the MIC should minimize its heat generation. Therefore, the qZSI module is very suitable for the outdoor application due to its high efficiency. When operated in an outdoor environment, the increased ambient temperature will lead to higher on-state resistance of the eGaN FETs, so the qZSI module efficiency could be slightly lower than the measured results in the laboratory[1][5].

V. CONCLUSION:

In this dissertation, We Design & Simulation Of High Performance Photovoltaic Module-Integrated Converter (MIC). Also Study Simulation of high new cost-effective and high-performance inverter topologies and advanced inverter for next generation PV systems. The cascaded structure reduced the voltage gain requirement of the MIC, so the front end eliminated dc-dc converter which is necessary in conventional MICs.the system reliability was also enhanced due to the qZSI shoot-through capability. The peak efficiency can be further improved to when the quasi-Z-source diode was replaced with SR. When the high-price eGaN devices are substituted with conventional Si-MOSFETs, the component cost can be reduced to half of the commercial PV MICs. The module can still achieve theoretical peak efficiency only less than –ve 0.5to –ve 0.75.

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